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4 Gb/s TWO-LEVEL TO 2 GSYMBOL/s FOUR-LEVEL CONVERTER GaAs IC FOR SEMICONDUCTOR OPTICAL AMPLIFIER MODULATORS

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ABSTRACT

For the first time a design of a 50 Ω impedance matched two-to-four level converter GaAs IC for two-electrode semiconductor optical amplifier modulators is presented. Eye diagrams with good eye openings and 0.33 V spacing between adjacent logic levels are demonstrated for input bit rates up to 4 Gb/s. A novel differential super buffer output driver is applied and output reflection coefficients $|S_{22}|$ of less than -12 dB for frequencies less than 10 GHz are obtained.

INTRODUCTION

Recently, semiconductor optical amplifiers (SOAs) have proven advantageous as optical modulators due to their high insertion gain (>10 dB fibre-to-fibre) and high modulation efficiency [1]. SOA modulators have two disadvantages in the form of a limited modulation speed and simultaneous generation of both AM and PM. The performance in terms of data rate can, however, be improved by a factor of two using four-level modulation. Furthermore, pure AM or PM can be achieved using differentially driven two-electrode SOAs [2]. A schematic diagram of such an improved modulator comprising a two-to-four level converter with differential outputs (D4L, $\overline{D4L}$) and a two-electrode SOA is shown in Fig.1. In this paper we present a full-custom designed two-to-four level converter GaAs IC, which is

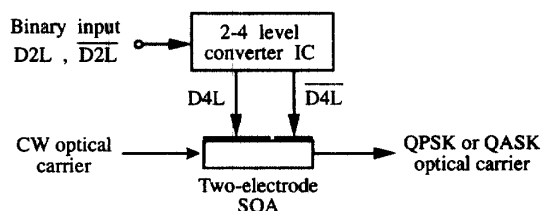


Fig.1. Schematic diagram of SOA modulator comprising the presented GaAs IC and a two-electrode SOA.

essential for implementation of the described scheme. With the presented converter the SOA modulator becomes efficient for use in optical QPSK and QASK microwave systems. In addition the developed encoder circuit principle will be advantageous in future long distance high speed optical fibre communication systems limited by fibre dispersion.

PRINCIPLE OF OPERATION

The designed two-to-four level converter transforms a two-level NRZ bit stream at bit rate B to a corresponding four-level signal at symbol rate B/2. It is composed of two main building blocks a 2-bit de-multiplexer (DMUX) and a two-to-four level encoder (TTFL) as shown in Fig.2. The de-multiplexer takes two consecutive bits (D1,D2) from the original two-level NRZ input bit stream (D2L) and applies them simultaneously to the input of the two-to-four level encoder. The encoder will then produce four different output voltage levels (D4L) corresponding to the four possible bit combinations of D1 and D2. All signals shown in Fig.2 are assumed to be differential.

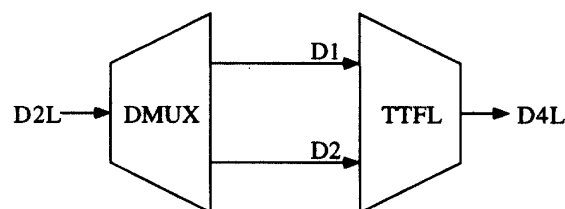


Fig.2. Block diagram of two-to-four level converter.

The encoder is realised by letting D1 and D2 control a pair of cross coupled current switches, which share the same resistive loads but steer currents differing a factor of two in magnitude as shown in Fig.3. From Fig.3 it is seen, that the combinations of voltage drops across the two resistive loads R_L corresponding to the four possible combinations of switch settings become $(3R_L I, 0)$, $(2R_L I, R_L I)$, $(R_L I, 2R_L I)$ and $(0, 3R_L I)$. The desired encoder function of generating differential four level output signals from D1 and D2 is thus obtained.

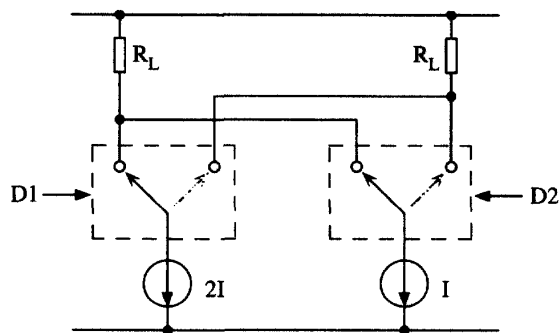


Fig.3. Block diagram of ideal two-to-four level encoder.

CIRCUIT DESIGN

The two-to-four level encoder and the output driver are implemented as being an integral part of each other as shown in Fig.4. It is seen, that the ideal switches and associated ideal current sources of the ideal encoder shown in Fig.3 have been replaced with differential amplifiers. Thus, the two-to-four level encoding is realised using two cross coupled differential amplifiers, which differ a factor of two in size but share the same loads. In this manner well defined differential four level signals are obtained at the gates of T_1 and T_2 . As mentioned above the two-to-four level encoder is implemented as an integral part of the output driver. This is done in order to minimise the number of stages succeeding the encoder and thereby to preserve the well defined logic levels. The converter is intended to drive an AC-coupled $50\ \Omega$ matched two-electrode SOA directly or alternatively via an AC-coupled $50\ \Omega$ amplifier. However, although the SOA and amplifier are impedance matched, the converter outputs should be impedance matched in order to reduce reflections in the final modulator set-up. Therefore the output driver is

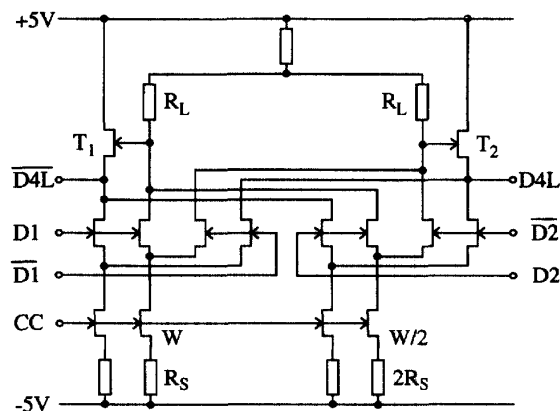


Fig.4. Circuit diagram of two-to-four level encoder.

implemented as the differential super buffer shown in Fig.4, which can be designed to provide $50\ \Omega$ output matching while driving an AC-coupled $50\ \Omega$ load. By proper design the currents through T_1 and T_2 will be nearly constant (10 mA) for the full range of output voltages ($2V \leq V_{D4L} \leq 3V$), and to a first order approximation the output impedances will then be constant and given by the inverse of the transconductances of T_1 and T_2 .

The performance of the developed differential super buffer output driver should be seen in view of the widely accepted open drain interfacing, which in its original form [3] can not drive AC loads, nor does it employ impedance matching at the output, which necessitates good impedance matching at the receiving end. Creating output matching by placing a $50\ \Omega$ resistor at the output of the transmitter will double the output driver power consumption and the size of the output transistors. This is often not acceptable. As a compromise designers have instead placed $100\ \Omega$ resistors at the transmitting end and have thereby obtained some impedance matching at high frequencies [4] but poor matching at low frequencies. Though the application of the output driver is very specific in our case, the authors believe, that the developed differential super buffer has a potential for chip-to-chip impedance matched high-speed interfacing at lower power dissipation than for existing configurations.

The logic gates employed in the 2-bit demultiplexer are designed using Source Coupled FET Logic (SCFL), which fits in naturally with the encoder sub-circuit topology. The final two-to-four level converter design has been processed in TriQuints $0.5\ \mu\text{m}$ gate length ($F_t=20\ \text{GHz}$) HA process. A micro photograph of the designed two-to-four level converter IC is shown in Fig.5.

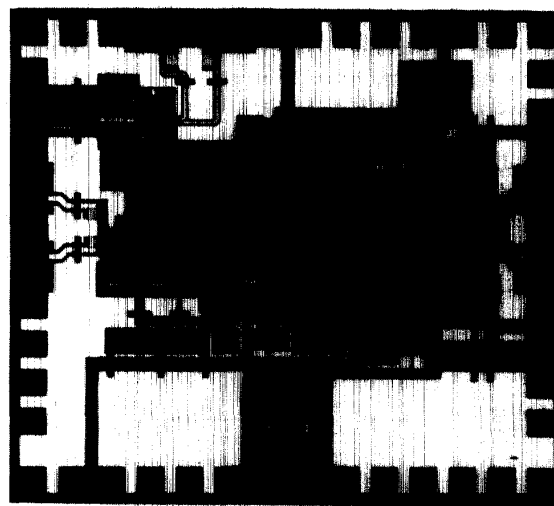


Fig.5. Micro photograph of two-to-four level converter IC.

MEASURED PERFORMANCE

The chips were tested using wafer probing. By applying PRBS data to the data input (D2L) and monitoring the outputs on a sampling oscilloscope correct encoding is observed at input bit rates exceeding 4 Gb/s corresponding to 2 Gsymbol/s at the output, see Fig.6. At input bit rates exceeding 4 Gb/s eye diagrams with good eye openings are observed, see Fig.7, but for input bit rates exceeding 4.5 Gb/s the eyes are almost closed. The chip operates equally well with outputs DC-terminated to 50 Ω /+2.5 V or AC-terminated to 50 Ω . In both cases the spacing between adjacent logic levels is 0.33 V. The output reflection coefficients $|S_{22}|$ corresponding to the lowest ($V_{D4L}=2$ V) and highest ($V_{D4L}=3$ V) logic output level have been measured. They are found to stay below -16 dB and -12 dB for frequencies below 1 GHz (corresponding to 2 Gsymbol/s) and 10 GHz, respectively, as shown in Fig.8.

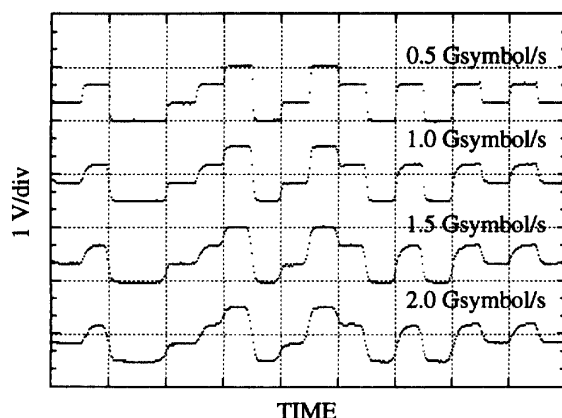


Fig.6. Measured output wave forms.

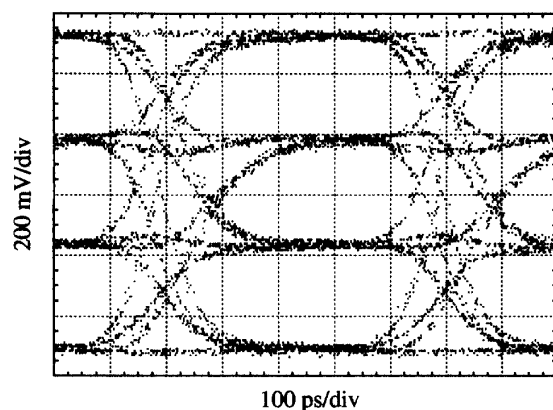


Fig.7. Measured output eye diagram at 2 Gsymbol/s.

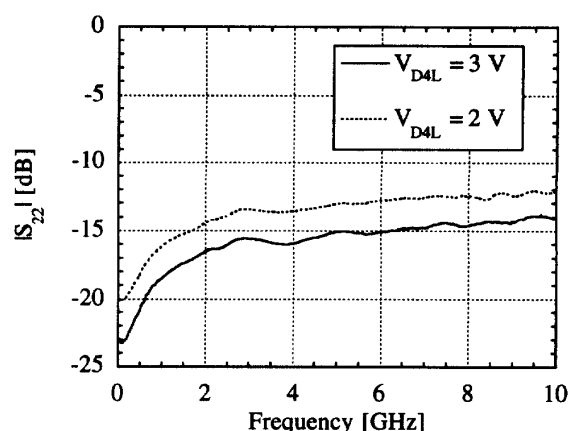


Fig.8. Measured output reflection coefficients $|S_{22}|$.

CONCLUSION

A two-to-four level converter GaAs IC for two-electrode semiconductor amplifier modulators has been designed. Eye diagrams with good eye openings and correct encoding have been demonstrated at input bit rates up to 4 Gb/s corresponding to an output symbol rate of 2 Gsymbol/s. Good output matching and output level definition have been obtained through a novel output driver design comprising both two-to-four level encoding and generation of high-speed 50 Ω matched differential outputs.

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